

FIG. 1

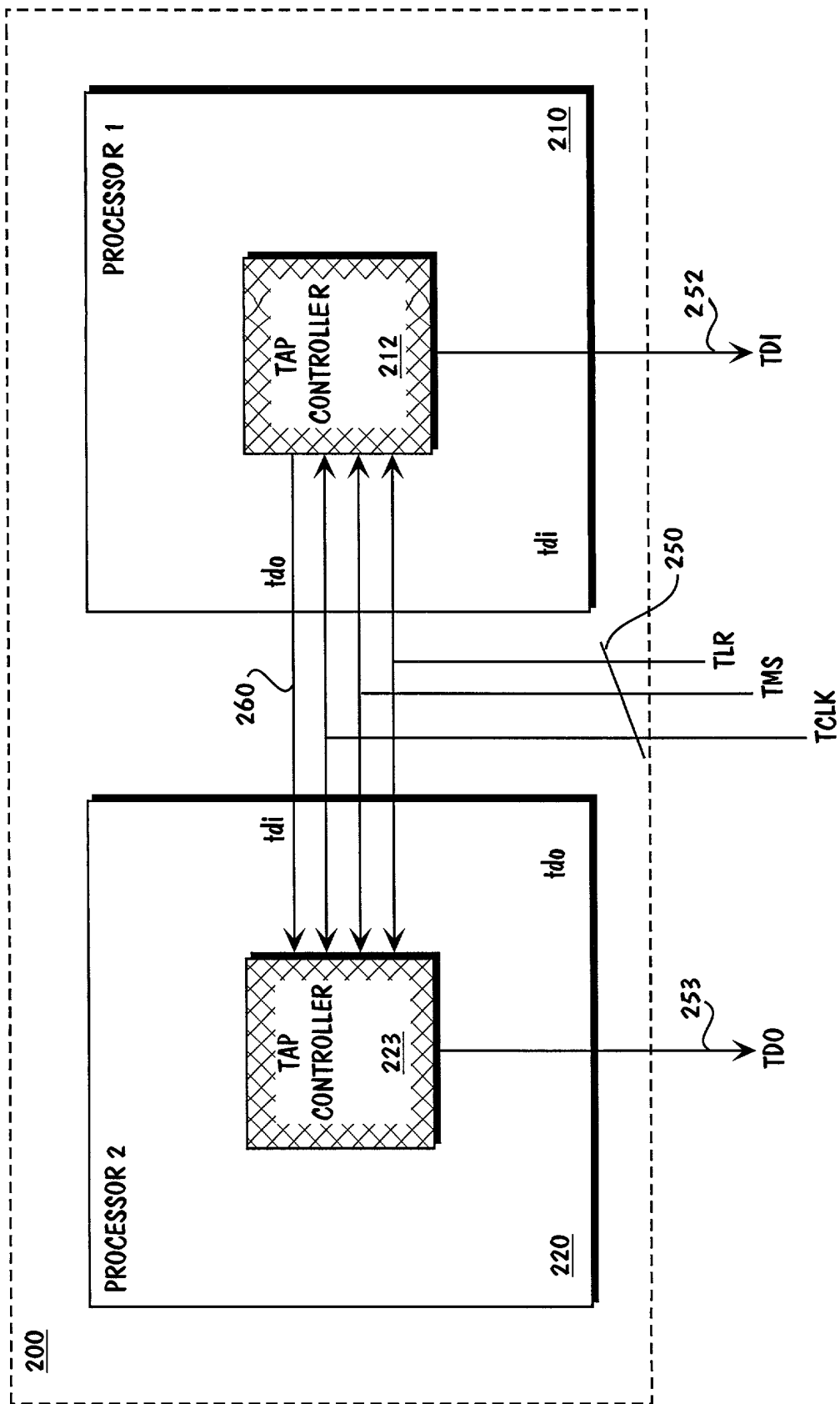


FIG. 2

FIG. 3a

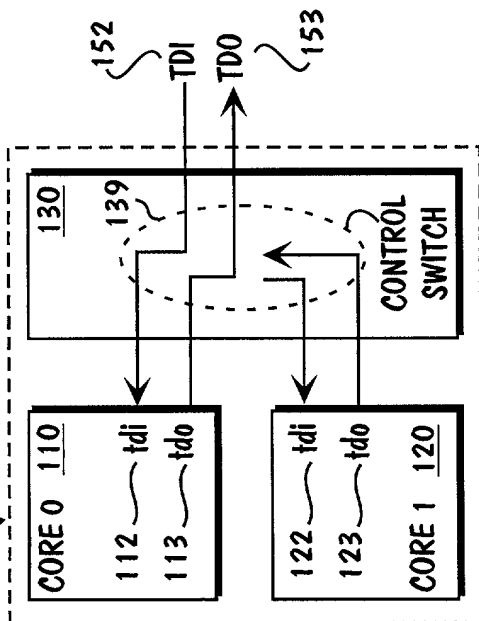


FIG. 3b

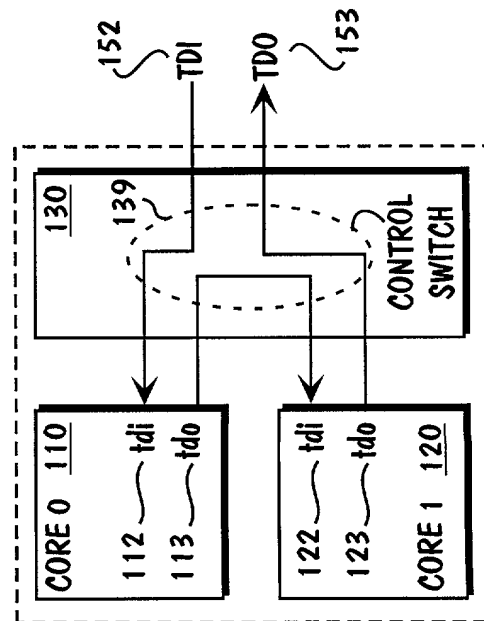
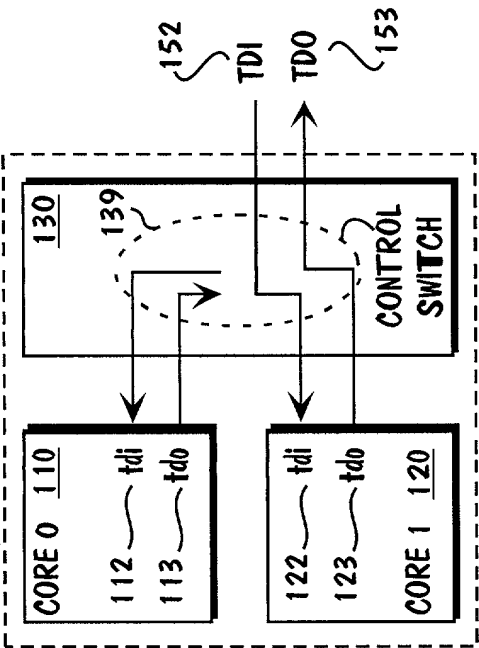


FIG. 3c

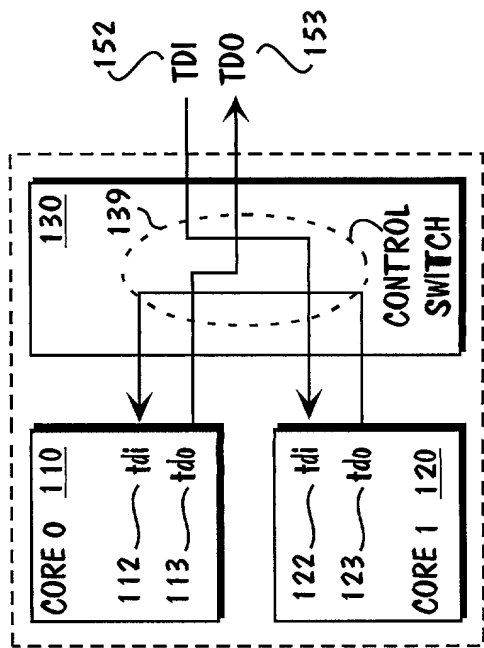


FIG. 3d

FIG. 4a

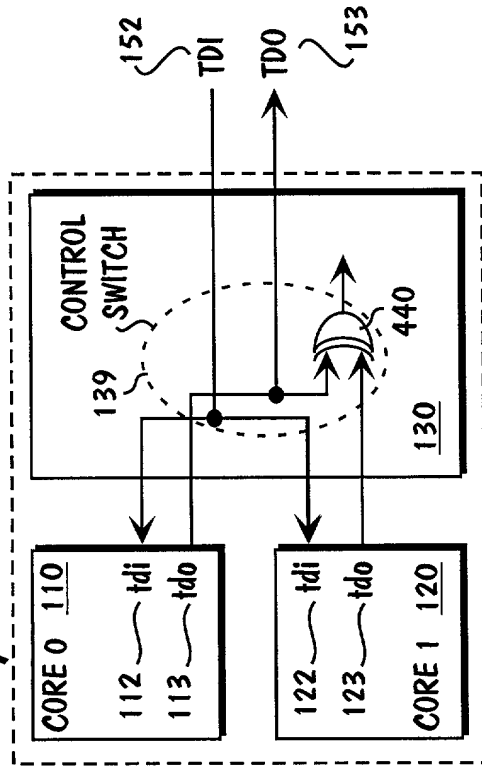


FIG. 4b

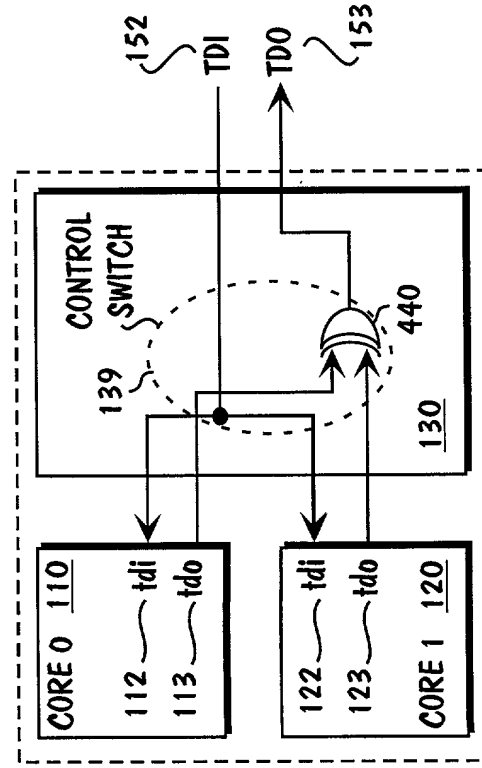
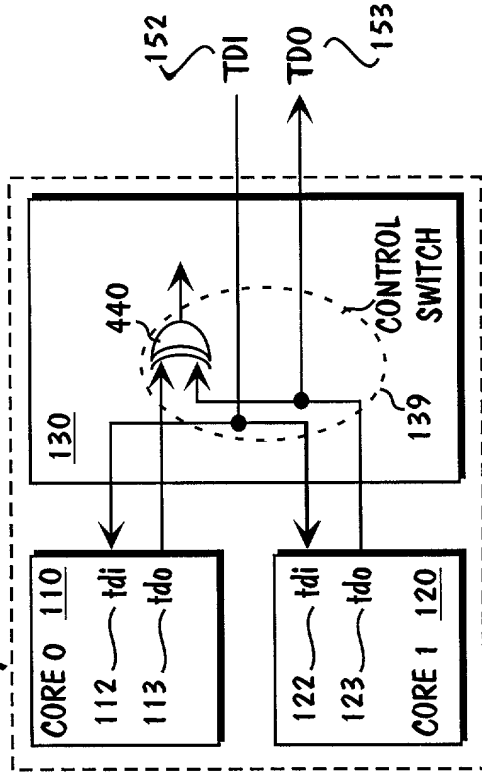


FIG. 4c

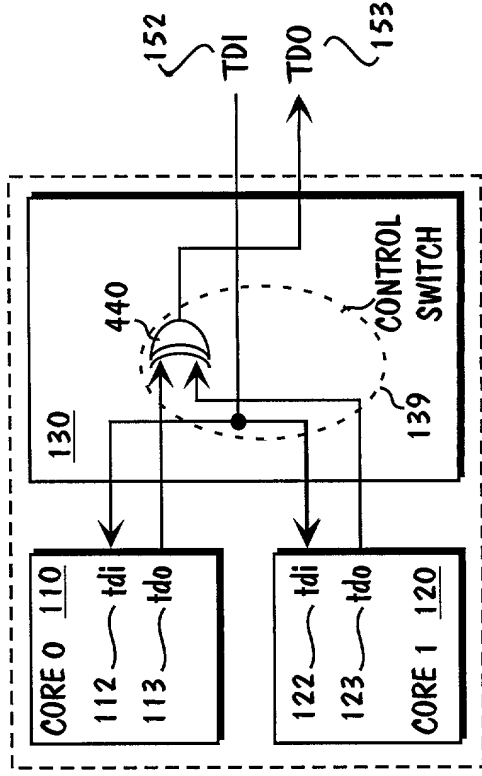


FIG. 4d

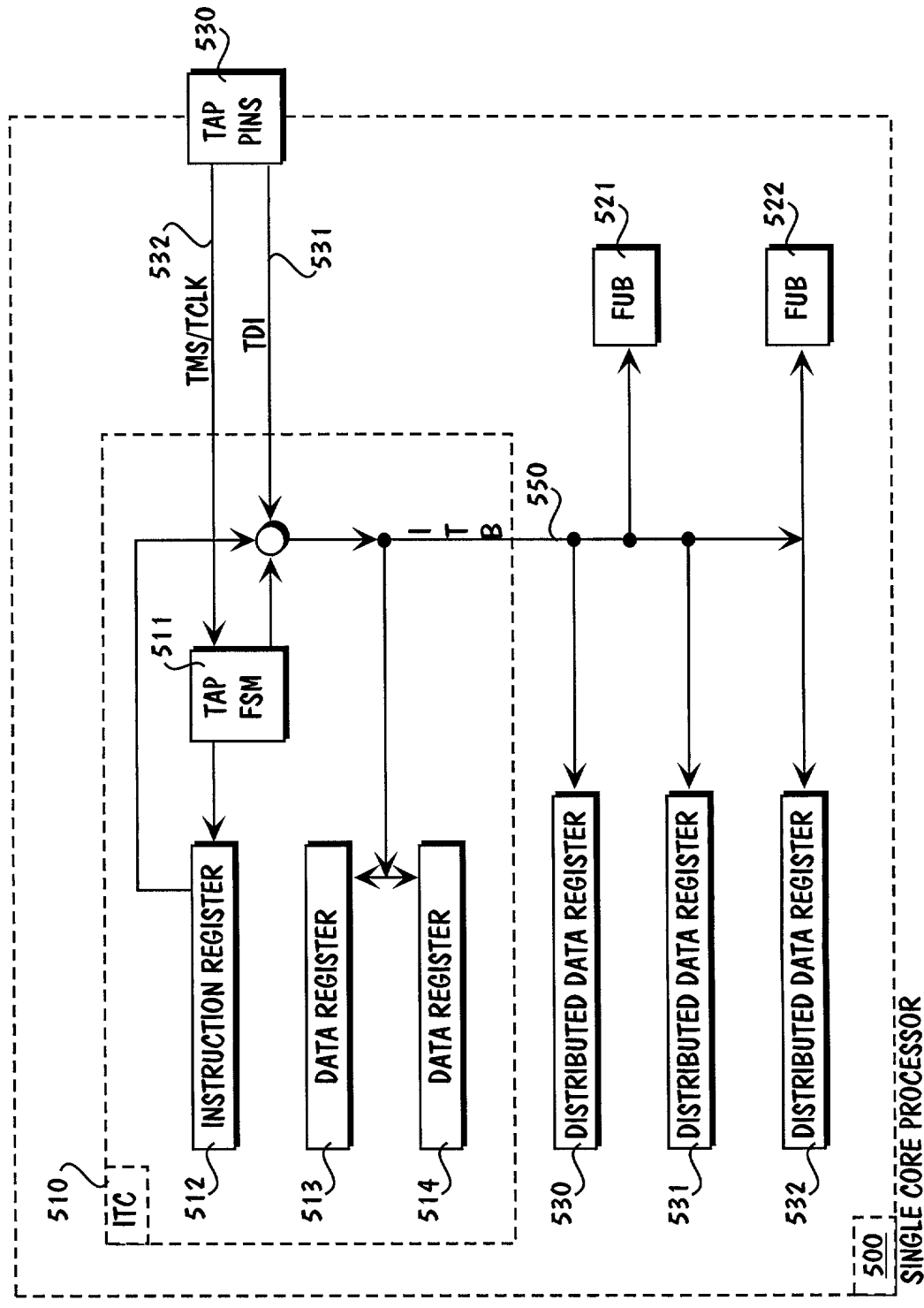


FIG. 5

INTEGRATED TEST BUS

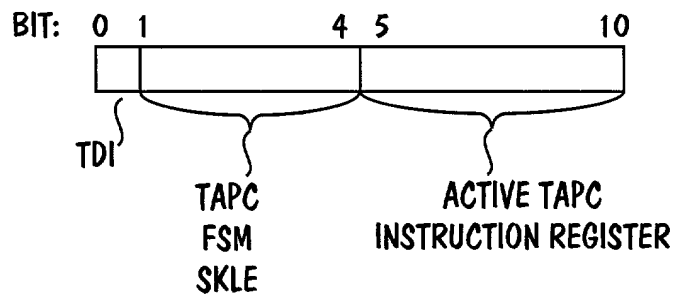


FIG. 6

TAP CORE CONFIGURATION REGISTER

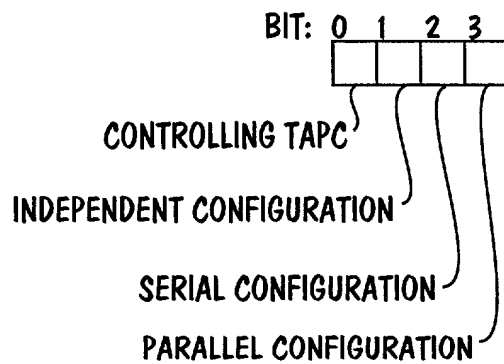


FIG. 7

FIG. 8

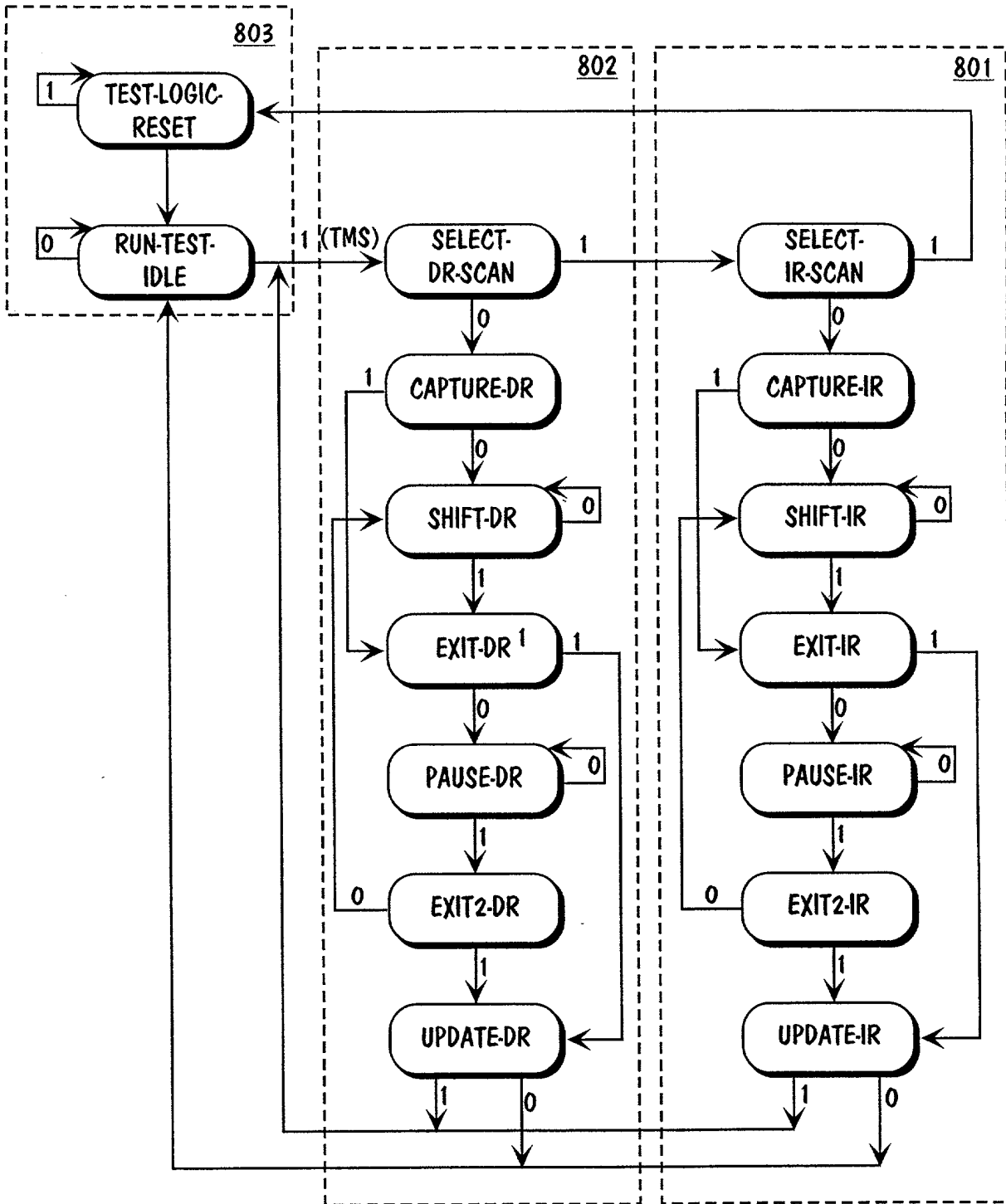


FIG. 8

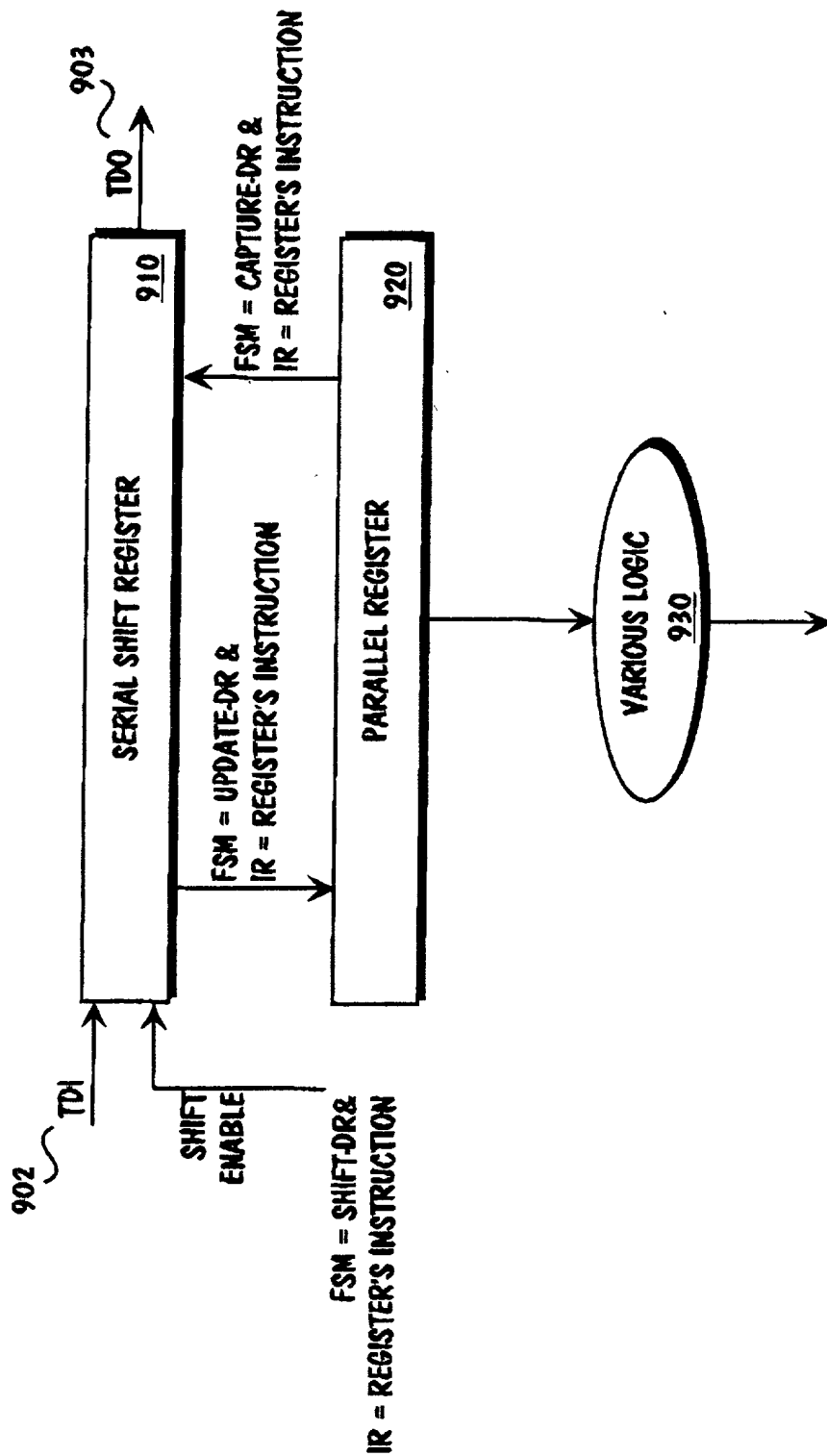


FIG. 9